IN THE CLAIMS:

Please amend claims 1, 2, 4, 7, 8, 10, 11, 16, and 17 as follows. Please cancel claims 9 and 18 without prejudice. Please add new claims 19-21.

1. (Currently Amended) A signal processor for Fast Fourier Transformation[[, FFT ,]] of M_R, $M_R > 1$, input data streams ~~(xl(n), ..., x4(n))~~ supplied in parallel, comprising:

[[-]] a multiplexing device ~~(MUX)~~ comprising ~~having~~ M_R input terminals each receiving one of the M_R input data streams, ~~(xl (n), ..., x4 (n))~~ and an output terminal ~~(x' (n))~~ at which the M_R input data streams are output in a multiplexed manner;[[,]]

[[-]] a Fast Fourier Transformation device ~~(FFT)~~ configured to perform Fast Fourier Transformation of a data stream supplied at an input terminal ~~(x' (n))~~ thereof and to output the ~~FFT~~ Fast Fourier Transformation transformed data stream at an output terminal ~~(X(k))~~ thereof, the input terminal of the Fast Fourier Transformation device ~~(FFT)~~ being connected to the output terminal ~~(X(n))~~ of the multiplexing device ~~(MUX)~~;[[,]] and

[[-]] a demultiplexing device ~~(DEMUX)~~ comprising ~~having~~ an input terminal connected to the output terminal ~~(X(k))~~ of the Fast Fourier Transformation device ~~(FFT)~~ and M_R output terminals ~~(Xl(k), ..., X4(k))~~ at which a respective one of M_R transformed output data streams is output in a demultiplexed manner, ~~characterized in that~~ wherein

[[-]] each of the M_R input data streams contains a number of $N=2^k$

samples,

[[-]] the Fast Fourier Transformation device ~~(FFT)~~ has a pipeline architecture composed of k stages with a respective feedback path including a single delay element per each stage of the pipeline architecture and is controlled by a first ~~(clk')~~ and second internal control signals ~~(s', t', w')~~,

~~wherein~~

the delay element in a feedback path of an i^{th} stage, $1<=i<=k$, of the pipeline architecture imposes a delay of $M_R*N/2^i$ samples,

the first internal control signal ~~(clk')~~ is clocked M_R times faster compared to a clock rate ~~(clk)~~ at which the samples of the M_R streams are supplied, and

the second internal control signals ~~(s', t', w')~~ are clocked M_R times slower compared to the first internal control signal ~~(cik')~~.

2. (Currently Amended) A signal processor according to claim 1, wherein

the multiplexing device ~~(MUX)~~ is configured such that the M_R input data streams are multiplexed per data sample of the input data streams, and

the demultiplexing device ~~(DEMUX)~~ is configured such that the transformed input data stream is demultiplexed per data sample of the transformed data stream.

3. (Original) A signal processor according to claim 2, wherein

a control signal supplied to the multiplexer and demultiplexer is clocked at a rate M_R times the clock rate of the supplied streams.

4. (Currently Amended) A signal processor according to claim 1, wherein

the Fast Fourier Transformation device ~~(FFT)~~ has a Radix-2 Single-path Delay Feedback[[, R^2SDF,]] architecture.

5. (Currently Amended) A signal processor according to claim 4, wherein the pipeline architecture of the Fast Fourier Transformation device is composed of Butterfly stages of types I and II ~~(BF2I, BF2II)~~.

6. (Original) A signal processor according to claim 5, wherein

the first stage of the pipeline architecture receiving the multiplexed data streams is a Butterfly stage of type I for even and odd total numbers of k.

7. (Currently Amended) A network element of a communication network, the network element comprising:

a signal processor according to ~~any of the preceding claims~~ claim 1 ~~to 6~~.

8. (Currently Amended) A terminal configured to communicate via a communication network, the terminal comprising a signal processor according to ~~any of the preceding claims~~ claim 1 ~~to 6~~.

9. (Canceled).

10. (Currently Amended) A signal processing method for performing Fast Fourier Transformation[[, FFT ,]] of M_R, $M_R > 1$, input data streams ~~(xl(n), ..., x_{MR}(n))~~ supplied in parallel, the method comprising: ~~the steps of~~

[[-]] multiplexing the M_R input data streams ~~(xl(n), ..., x_{MR}(n))~~ to a multiplexed data stream;[[,]]

[[-]] performing Fast Fourier Transformation of the multiplexed data stream and outputting the transformed data stream;[[,]]

[[-]] demultiplexing the transformed data stream to M_R transformed output data streams, ~~characterized by~~ wherein[[-]] each of the M_R input data streams contains a number of $N=2^k$ samples;[[,]]

[[-]] performing ~~FFT~~ Fast Fourier Transformation ~~transformation~~ using a pipeline of k stages with a respective feedback path imposing a delay on the samples per each stage of the pipeline; ~~and~~

[[-]] controlling the performing of the ~~FFT~~ Fast Fourier Transformation ~~transformation~~ by a first ~~(clk')~~ and second internal control signals ~~(s', t', w')~~[[-]] and by imposing a delay of $M_R*N/2^i$ samples on the samples in the feedback path of an i^{th} stage, $1<=i<=k$, of the pipeline;[[,]]

clocking the first internal control signal ~~(clk')~~ M_R times faster compared to a clock rate ~~(clk)~~ at which the samples of the M_R streams are supplied;[[,]] and

clocking the second internal control signals ~~(s', t', w')~~ M_R times slower compared to the first internal control signal ~~(clk')~~.

11. (Currently Amended) A method according to claim 10, wherein

multiplexing is accomplished such that the M_R input data streams are multiplexed per data sample of the input data streams, and

demultiplexing is accomplished such that the transformed data stream is demultiplexed per data sample of the transformed data stream.

12. (Original) A method according to claim 11, wherein

clocking to the multiplexer and demultiplexer is performed at a rate M_R times the clock rate of the supplied streams.

13. (Original) A method according to claim 10, wherein

the Fast Fourier Transformation processing is based on a Radix-2 Single-path Delay Feedback algorithm.

14. (Currently Amended) A method according to claim 13, wherein

the pipeline of processing stages for the Fast Fourier Transformation is composed of Butterfly stages of types I and II ~~(BF2I, BF2II)~~.

15. (Original) A method according to claim 14, wherein

the first stage of the pipeline receiving the multiplexed data stream is a Butterfly stage of type I for even and odd total numbers of k.

16. (Currently Amended) A computer chip comprising at least a signal processor according to ~~any of the preceding claims~~ claim 1 ~~to 6~~.

17. (Currently Amended) A computer program, embodied on a machine-readable medium, said computer program controlling a computer device to: ~~product for a computer, comprising software code portions for performing the steps of any one of claims 10 to 15 when the program is run on the computer~~

multiplex the M_R input data streams to a multiplexed data stream;

perform Fast Fourier Transformation of the multiplexed data stream and outputting the transformed data stream;

demultiplex the transformed data stream to M_R transformed output data streams, wherein each of the M_R input data streams contains a number of $N=2^k$ samples;

perform Fast Fourier Transformation using a pipeline of k stages with a respective feedback path imposing a delay on the samples per each stage of the pipeline;

control the performing of the Fast Fourier Transformation by a first and second internal control signals and by imposing a delay of $M_R*N/2^i$ samples on the samples in the feedback path of an i^{th} stage, $1<=i<=k$, of the pipeline;

clock the first internal control signal M_R times faster compared to a clock rate at which the samples of the M_R streams are supplied; and

clock the second internal control signals M_R times slower compared to the first internal control signal.

18. (Cancelled).

19. (New) A signal processor for Fast Fourier Transformation of M_R, M_R>1, input data streams supplied in parallel, comprising:

multiplexing means for multiplexing the M_R input data streams to a multiplexed data stream;

first Fast Fourier Transformation means for performing Fast Fourier Transformation of the multiplexed data stream and outputting the transformed data stream;

demultiplexing means for demultiplexing the transformed data stream to M_R transformed output data streams, wherein each of the M_R input data streams contains a number of $N=2^k$ samples;

second Fast Fourier Transformation means for performing Fast Fourier Transformation using a pipeline of k stages with a respective feedback path imposing a delay on the samples per each stage of the pipeline;

controlling means for controlling the performing of the Fast Fourier Transformation by a first and second internal control signals and by imposing a delay of $M_R*N/2^i$ samples on the samples in the feedback path of an i^{th} stage, 1<=i<=k, of the pipeline;

first clocking means for clocking the first internal control signal M_R times

faster compared to a clock rate at which the samples of the M_R streams are supplied; and

second clocking means for clocking the second internal control signals M_R times slower compared to the first internal control signal.

20. (New) A system comprising:

a terminal configured to communicate via a communication network, the terminal comprising a signal processor for Fast Fourier Transformation of M_R, $M_R>1$, input data streams supplied in parallel,

wherein the signal processor comprises

a multiplexing device comprising M_R input terminals each receiving one of the M_R input data streams, and an output terminal at which the M_R input data streams are output in a multiplexed manner;

a Fast Fourier Transformation device configured to perform Fast Fourier Transformation of a data stream supplied at an input terminal thereof and to output the Fast Fourier Transformation transformed data stream at an output terminal thereof, the input terminal of the Fast Fourier Transformation device being connected to the output terminal of the multiplexing device; and

a demultiplexing device comprising an input terminal connected to the output terminal of the Fast Fourier Transformation device and M_R output terminals at which a respective one of M_R transformed output data streams is output in a demultiplexed manner, wherein

each of the M_R input data streams contains a number of $N=2^k$

samples,

the Fast Fourier Transformation device has a pipeline architecture composed of k stages with a respective feedback path including a single delay element per each stage of the pipeline architecture and is controlled by a first and second internal control signals,

the delay element in a feedback path of an i^{th} stage, $1<=i<=k$, of the pipeline architecture imposes a delay of $M_R*N/2^i$ samples,

the first internal control signal is clocked M_R times faster compared to a clock rate at which the samples of the M_R streams are supplied, and

the second internal control signals are clocked M_R times slower compared to the first internal control signal.

21. (New) A system comprising:

a network element, the network element comprising a signal processor for Fast Fourier Transformation of M_R, $M_R>1$, input data streams supplied in parallel,

wherein the signal processor comprises

a multiplexing device comprising M_R input terminals each receiving one of the M_R input data streams, and an output terminal at which the M_R input data streams are output in a multiplexed manner;

a Fast Fourier Transformation device configured to perform Fast Fourier Transformation of a data stream supplied at an input terminal thereof and to output the Fast Fourier Transformation transformed data stream at an output

terminal thereof, the input terminal of the Fast Fourier Transformation device being connected to the output terminal of the multiplexing device; and

a demultiplexing device comprising an input terminal connected to the output terminal of the Fast Fourier Transformation device and M_R output terminals at which a respective one of M_R transformed output data streams is output in a demultiplexed manner, wherein

each of the M_R input data streams contains a number of $N=2^k$ samples,

the Fast Fourier Transformation device has a pipeline architecture composed of k stages with a respective feedback path including a single delay element per each stage of the pipeline architecture and is controlled by a first and second internal control signals,

the delay element in a feedback path of an i^{th} stage, $1<=i<=k$, of the pipeline architecture imposes a delay of $M_R*N/2^i$ samples,

the first internal control signal is clocked M_R times faster compared to a clock rate at which the samples of the M_R streams are supplied, and

the second internal control signals are clocked M_R times slower compared to the first internal control signal.